Test format for Annexure- I

## Issuance of certificate of fitness of solar power generation system (SPGS)

Consumer Name Consumer No Address Test for Details Of Solar PV Ge		ection / Periodic checking	(✔the appr					
Address Test for	: New Conne	ection / Periodic checking	(✔the appr					
Test for	: New Conne	ection / Periodic checking	( the appro					
		ection / Periodic checking	( the appro					
Details Of Solar PV Ge				opriate )				
	enerator							
Solar Module Model N	No .:	Make .:		No. of Mo	odules :		Total Cap	pacity:
					l Capacity :			
nverter Details :		Make :			Model No.			
AC Capacity of Inverte		GPS ( Up	GPS ( Up To 6 Decimal Places ) :					
Inverter Serial No.			200		ackup : Yes /No attery :	200	propriate)	
a) Anti-Island Voltage at t Voltage at Anti – Island	ling Test (As per IEC the inverter terminal inverter terminal ding (As per IEC 62	2116/ IEC 61727)	for testing p : : OK/ NOT (	urpose ) : R-N : OK ( ✓ the a	R-N : Y-I	N :	. B-N :	
a) Anti -Island Voltage at t Voltage at Anti – Island 7 THD In Voltage - Me	ding Test (As per IEC the inverter termin inverter terminal ding (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure	I for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N : DK (  the a	: R-N : Y-I Y-N : appropriate)	N :	. B-N :	
a) Anti-Island Voltage at t Voltage at Anti – Island 6 THD In Voltage - Me Permissible Voltage Dis	ding Test (As per IEC the inverter terminal inverter terminal ding (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N: DK ( v the a ion : Voltage	R-N : Y-I Y-N : appropriate)	N : B-N :	. B-N :	
a) Anti -Island Voltage at t Voltage at Anti – Island 6 THD In Voltage - Me Permissible Voltage Dis As per IEEE 519 :2014)	ding Test (As per IEC the inverter terminal inverter terminal ding (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N: DK ( \( \nabla \) the a ion : Voltage	R-N: Y-I 	N : B-N :	. B-N :	
a) Anti-Island Voltage at t Voltage at Anti – Island 6 THD In Voltage - Me ermissible Voltage Dis As per IEEE 519 :2014)	ding Test (As per IEC the inverter terminal inverter terminal ding (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N:  DK (  the a ion : Voltage  /oltage L	R-N:Y-I Y-N: appropriate)  Distortion  evel:	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at Anti – Island THD In Voltage - Me ermissible Voltage Dis s per IEEE 519 :2014) Voltage Level	ding Test (As per IEC the inverter terminal inverter terminal ing (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N:  DK (  the a ion : Voltage  /oltage L	R-N: Y-I 	N : B-N :	. B-N :	
a) Anti-Island Voltage at t Voltage at Anti-Island Anti-Island The Island The	ding Test (As per IEC the inverter terminal inverter terminal ding (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N:  DK (  the a ion : Voltage  /oltage L	R-N:Y-I Y-N: appropriate)  Distortion  evel:	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at t Anti-Island STHD In Voltage - Me ermissible Voltage Dis As per IEEE 519 :2014) Voltage Level V<1.0 KV LKV <v<=69kv< td=""><td>ding Test (As per IEC the inverter terminal inverter terminal ing (As per IEC 62 easured at</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT ( ad –off condit</td><td>urpose) : R-N:  DK (  the a ion : Voltage  /oltage L</td><td>R-N:Y-I Y-N: appropriate)  Distortion  evel:</td><td>N:B-N:</td><td>. B-N :</td><td></td></v<=69kv<>	ding Test (As per IEC the inverter terminal inverter terminal ing (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N:  DK (  the a ion : Voltage  /oltage L	R-N:Y-I Y-N: appropriate)  Distortion  evel:	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at Anti – Island 6 THD In Voltage - Me Permissible Voltage Dis As per IEEE 519 :2014) Voltage Level V<1.0 KV 1KV <v<=69kv< td=""><td>ding Test (As per IEC the inverter terminal inverter inve</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT ( ad –off condit</td><td>urpose) : R-N:  DK (  the a ion : Voltage  /oltage L</td><td>R-N:Y-I Y-N: appropriate)  Distortion  evel:</td><td>N:B-N:</td><td>. B-N :</td><td></td></v<=69kv<>	ding Test (As per IEC the inverter terminal inverter inve	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N:  DK (  the a ion : Voltage  /oltage L	R-N:Y-I Y-N: appropriate)  Distortion  evel:	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at t Anti – Island % THD In Voltage - Me Permissible Voltage Dis As per IEEE 519 :2014)  Voltage Level V<1.0 KV  1KV <v<=69kv 59="" kv<="" kv<v<="161" td=""><td>ding Test (As per IEC the inverter terminal inverter inve</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT ( ad –off condit</td><td>urpose) : R-N:  DK (  the a ion : Voltage  /oltage L</td><td>R-N:Y-I Y-N: appropriate)  Distortion  evel:</td><td>N:B-N:</td><td>. B-N :</td><td></td></v<=69kv>	ding Test (As per IEC the inverter terminal inverter inve	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N:  DK (  the a ion : Voltage  /oltage L	R-N:Y-I Y-N: appropriate)  Distortion  evel:	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at t Anti – Island % THD In Voltage - Me Permissible Voltage Dis As per IEEE 519 :2014)  Voltage Level V<1.0 KV  1KV <v<=69kv 59="" kv<="" kv<v<="161" td=""><td>ding Test (As per IEC the inverter terminal inverter inve</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT ( ad –off condit</td><td>urpose) : R-N:  DK (  the a ion : Voltage  /oltage L</td><td>R-N:Y-I Y-N: appropriate)  Distortion  evel:</td><td>N:B-N:</td><td>. B-N :</td><td></td></v<=69kv>	ding Test (As per IEC the inverter terminal inverter inve	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT ( ad –off condit	urpose) : R-N:  DK (  the a ion : Voltage  /oltage L	R-N:Y-I Y-N: appropriate)  Distortion  evel:	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at t Anti – Island 6 THD In Voltage - Me Permissible Voltage Dis As per IEEE 519 :2014) Voltage Level V<1.0 KV 1KV <v<=69kv 19="" by="" cower="" generated="" in="" inver<="" kv<v<="161" td="" the="" vailable=""><td>ding Test (As per IEC the inverter terminal inverter display panel inverter display panel</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT 0 ad −off condit V R-N Not Ok(✓ ap</td><td>urpose) : R-N:</td><td>Particular Representation  Distortion  Evel:  THD (%) Mea</td><td>N:B-N:</td><td>. B-N :</td><td></td></v<=69kv>	ding Test (As per IEC the inverter terminal inverter display panel inverter display panel	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT 0 ad −off condit V R-N Not Ok(✓ ap	urpose) : R-N:	Particular Representation  Distortion  Evel:  THD (%) Mea	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at t Anti – Island 6 THD In Voltage - Me ermissible Voltage Dis As per IEEE 519 :2014) Voltage Level V<1.0 KV LKV <v<=69kv 9="" by="" generated="" in="" inver<="" kv<v<="161" ower="" td="" the="" v="" vailable=""><td>ding Test (As per IEC the inverter terminal inverter (As per IEC 62 easured at</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT 0 ad −off condit  V  R-N  Not Ok(✓ ap</td><td>urpose) :: R-N:</td><td>Particular Representation  Distortion  Evel:  THD (%) Mea</td><td>N:B-N:</td><td>. B-N :</td><td></td></v<=69kv>	ding Test (As per IEC the inverter terminal inverter (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT 0 ad −off condit  V  R-N  Not Ok(✓ ap	urpose) :: R-N:	Particular Representation  Distortion  Evel:  THD (%) Mea	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at t Voltage at Anti – Island THD In Voltage - Me THD In Voltage Dis As per IEEE 519 :2014)  Voltage Level V<1.0 KV  LKV <v<=69kv 9="" by="" generated="" in="" inver<="" kv<v<="161" ower="" td="" the="" v="" vailable=""><td>ding Test (As per IEC the inverter terminal inverter terminal iding (As per IEC 62 easured at</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT 0 ad –off condit  V  R-N  Not Ok(  ap  Watt  he appropriat</td><td>urpose) :: R-N:</td><td>Particular Representation  Distortion  Evel:  THD (%) Mea</td><td>N:B-N:</td><td>. B-N :</td><td></td></v<=69kv>	ding Test (As per IEC the inverter terminal inverter terminal iding (As per IEC 62 easured at	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT 0 ad –off condit  V  R-N  Not Ok(  ap  Watt  he appropriat	urpose) :: R-N:	Particular Representation  Distortion  Evel:  THD (%) Mea	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at t Voltage at t Anti – Island 6 THD In Voltage - Me Permissible Voltage Dis As per IEEE 519 :2014)  Voltage Level V<1.0 KV  1KV <v<=69kv (during="" 9="" by="" generated="" in="" invertent="" isolation="" kv<v<="161" manual="" observations="" other="" re<="" solution)="" spgs="" switch="" td="" the="" vailable="" vower=""><td>ding Test (As per IEC the inverter terminal inverter discourse as under the for battery backulemarks (if any)</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT 0 ad –off condit  V  R-N  Not Ok(  ap  Watt  he appropriat</td><td>urpose) :: R-N:</td><td>Particular Representation  Distortion  Evel:  THD (%) Mea</td><td>N:B-N:</td><td>. B-N :</td><td></td></v<=69kv>	ding Test (As per IEC the inverter terminal inverter discourse as under the for battery backulemarks (if any)	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT 0 ad –off condit  V  R-N  Not Ok(  ap  Watt  he appropriat	urpose) :: R-N:	Particular Representation  Distortion  Evel:  THD (%) Mea	N:B-N:	. B-N :	
a) Anti-Island Voltage at t Voltage at t Voltage at t Anti – Island % THD In Voltage - Me Permissible Voltage Dis (As per IEEE 519 :2014)  Voltage Level V<1.0 KV  1KV <v<=69kv 59="" available="" by="" c<="" content="" generated="" in="" invertion="" kv="" kv<v<="161" of="" power="" td="" the=""><td>ding Test (As per IEC the inverter terminal inverter discourse as under the for battery backuremarks (if any)</td><td>C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT 0 ad −off condit  V  R-N  Not Ok(✓ ap  Watt </td><td>urpose) :: R-N :</td><td>Part Representation Properties Pr</td><td>n: B-N: asured B-N</td><td>. B-N :</td><td></td></v<=69kv>	ding Test (As per IEC the inverter terminal inverter discourse as under the for battery backuremarks (if any)	C 62116/ IEC 61727 ): al (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT 0 ad −off condit  V  R-N  Not Ok(✓ ap  Watt	urpose) :: R-N :	Part Representation Properties Pr	n: B-N: asured B-N	. B-N :	
a) Anti-Island Voltage at t Voltage at t Voltage at t Anti – Island % THD In Voltage - Me Permissible Voltage Dis (As per IEEE 519 :2014)  Voltage Level V<1.0 KV  1KV <v<=69kv (during="" 59="" available="" by="" co<="" content="" generated="" in="" inver="" kv="" kv<v<="161" of="" power="" rrent="" second="" spgs="" td="" the=""><td>ding Test (As per IEC the inverter terminal inverter display particular inverter display panel in SPGS ON without I in for battery backulemarks (if any)</td><td>C 62116/ IEC 61727 ): cal (with grid synchronised after grid failure 2116/ IEC 61727)</td><td>d for testing p : : OK/ NOT 0 ad −off condit  V  R-N  Not Ok(✓ ap  Watt </td><td>urpose) :: R-N :</td><td>Part Representation  Distortion  Evel:  THD (%) Meany Part Representation  Ty-N  Ty-N  Ty:</td><td>n: B-N: asured B-N</td><td>. B-N :</td><td></td></v<=69kv>	ding Test (As per IEC the inverter terminal inverter display particular inverter display panel in SPGS ON without I in for battery backulemarks (if any)	C 62116/ IEC 61727 ): cal (with grid synchronised after grid failure 2116/ IEC 61727)	d for testing p : : OK/ NOT 0 ad −off condit  V  R-N  Not Ok(✓ ap  Watt	urpose) :: R-N :	Part Representation  Distortion  Evel:  THD (%) Meany Part Representation  Ty-N  Ty-N  Ty:	n: B-N: asured B-N	. B-N :	

- Single line diagram schematic diagram (to be furnished by the customer ): Yes / No a)
- b) Manufacturer's test certificates (to be furnished by the customer) : Yes/No

N.B.: Empanelled third party agency has carried out the test / The eligible consumer carried out the test in Presence of WBSEDCL's Representative .